

Code No: 153CK

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

B. Tech II Year I Semester Examinations, April/May - 2023

DIGITAL ELECTRONICS

(Computer Science and Design)

Time: 3 Hours

Max. Marks: 75

Note: i) Question paper consists of Part A, Part B.

ii) Part A is compulsory, which carries 25 marks. In Part A, Answer all questions.

iii) In Part B, Answer any one question from each unit. Each question carries 10 marks and may have a, b as sub questions.

PART – A**(25 Marks)**

- 1.a) Define the term diffusion capacitance C_D of a PN diode. [2]
- b) Define the term Transformer Utilization Factor (TUF) and PIV. [3]
- c) Define stability factor. [2]
- d) List the factors causing thermal runaway. [3]
- e) State De Morgans Laws. [2]
- f) Differentiate between J-FET and MOSFET. [3]
- g) Determine the complement of the AB $(BC'+BC)(AC'+AB)$. [2]
- h) What do you mean by K-map? Mention its advantages. [3]
- i) What is a sequential logic circuit? [2]
- j) Mention the differences between RAM and ROM. [3]

PART – B**(50 Marks)**

- 2.a) Explain the construction and working of photodiode.
- b) What is a clipping circuit? Explain the operation of a Positive clipper with suitable diagrams. [5+5]

OR

- 3.a) Explain the working of a full wave bridge rectifier with circuit diagram and input output waveforms.
- b) Explain the working of a Half wave rectifier with Capacitor filter and derive the expression for its ripple factor. [5+5]

- 4.a) What is the Thermal Runway? How can it be avoided?
- b) Explain the input and output characteristics of a transistor in CE configuration. [5+5]

OR

- 5.a) Draw the circuit diagram of a RC coupled amplifier and explain its operation.
- b) Compare the performance of a transistor in all the three configurations. [5+5]

6. Explain the construction and working of a depletion type MOSFET and compare it with enhancement type. [10]

OR

7. With suitable diagrams, explain the operation of a basic logic gates in RTL and DCTL logic. [10]

8. Define the function of a decoder. Design a 3 to 8 decoder, draw the circuit diagram, function table and explain the working of the decoder circuit. [10]

OR

9. Simplify the following function and implement it with NAND gates only. [10]

$$F' = (B' + D')(A' + C' + D)(A + B' + C' + D)(A' + B + C' + D')$$

10.a) Draw the circuit of JK Flip Flop using NAND gates and explain its operation.

b) Construct a T-flip-flop and explain its operation with truth and transition tables. [5+5]

OR

11.a) What is a shift register? Draw the block diagram and timing diagram of a shift register that shows the serial transfer of information from register A to register B.

b) Compare latches and flip flops. [6+4]

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Used papers 2023