

Code No: 183AP

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

B. Tech II Year I Semester Examinations, February - 2024

DIGITAL ELECTRONICS

(Computer Science and Engineering-IOT)

Time: 3 Hours

Max. Marks: 60

Note: This question paper contains two parts A and B.i) **Part- A** for 10 marks, ii) **Part - B** for 50 marks.

- Part-A is a compulsory question which consists of ten sub-questions from all units carrying equal marks.
- Part-B consists of **ten questions** (numbered from 2 to 11) **carrying 10 marks each**. From each unit, there are two questions and the student should answer one of them. Hence, the student should answer five questions from Part-B.

PART- A**(10 Marks)**

- 1.a) Find the equivalent Gray code for $[10110]_2$. [1]
- b) Outline the concept of duality in Boolean algebra. [1]
- c) What are don't care terms? [1]
- d) Prove that the logical sum of all minterms of a Boolean function of 2 variables is 1 [1]
- e) How does a 1-bit comparator work? [1]
- f) State the concept of parallel binary adder. [1]
- g) Mention any two differences between the edge triggering and level triggering. [1]
- h) What is sequential circuit? Give some example. [1]
- i) Distinguish between critical race and non-critical race. [1]
- j) List the different techniques used in State assignment. [1]

PART - B**(50 Marks)**

- 2.a) Minimize the following Boolean expressions using Boolean Algebra and draw the logic diagram $\bar{X}\bar{Y}Z + \bar{X}YZ + X\bar{Y}$.
- b) Perform the BCD addition of 375 and -267. [5+5]

OR

- 3.a) What are universal logic gates? Implement Ex-OR gate using Universal Logic gates.
- b) Obtain 3 level NOR – NOR implementation of $f = [ab + cd] ef$. [5+5]

4. Using K-map method, Simplify the following Boolean function and obtain
 - (a) minimal SOP and
 - (b) minimal POS expression & realize using only NAND and NOR gates $F = \sum m(0,2,3,6,7) + d(8,10,11,15)$. [5+5]

OR

5. Simplify the following function using K – map, $f = ABCD + AB'C'D' + AB'C + AB$ and realize the SOP using only NAND gates and POS using only NOR gates. [10]

- 6.a) Draw and explain the operation of full adder.
 b) Explain the operation of 4×1 multiplexer using suitable diagram. [5+5]

OR

7. Draw the logic diagram of BCD to Decimal decoder and explain its operations. [10]
 8. Design a synchronous 3-bit counter which counts in the sequence 1, 3, 2, 6, 7, 5, 4, (repeat) 1,3..... using T FF. [10]

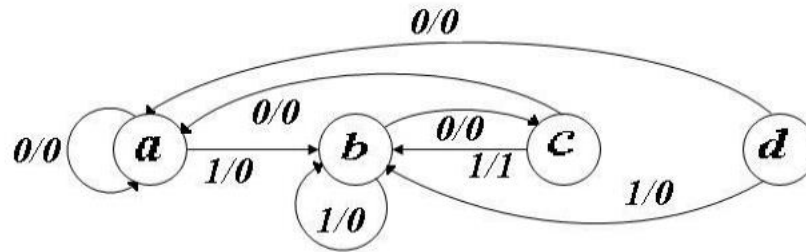
OR

9. Draw the logic diagram for a 5- bit serial load shift register using D FF and explain.[10]

- 10.a) Classify the methods of Race Free State assignment and explain in detail.
 b) Explain the different methods of state assignment. [5+5]

OR

11. Design a clocked sequential machine using JK flip flops for the state diagram shown in figure. Use state reduction if possible and make proper state assignment. [10]



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