Code No: 155CF **R18**

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
B. Tech III Year I Semester Examinations, August/September - 2024
MICROPROCESSORS AND MICROCONTROLLERS
(Common to ECM, CSE(IOT))

Time: 3 Hours **Max. Marks: 75**

Note: i) Question paper consists of Part A, Part B.
ii) Part A is compulsory, which carries 25 marks. In Part A, Answer all questions.
iii) In Part B, Answer any one question from each unit. Each question carries 10 marks and may have a, b as sub questions.

PART – A

(25 Marks)

1.a) What is the programming model of the 8086 microprocessors? [2]
b) Define the interrupt structure of the 8086 microprocessors. [3]
c) What is the role of I/O ports in microcontroller? [2]
d) Differentiate between timers and counters in the 8051 microcontroller, highlighting their specific functionalities. [3]
e) How does the SPI bus facilitate communication between the 8051 microcontroller and peripheral devices? [2]
f) What is the purpose of the UART in the 8051 microcontroller? [3]
g) How are branch instructions utilized in ARM architecture for program flow control? [2]
h) Define load/store instructions in ARM and their role in memory data access. [3]
i) Compare the memory architecture of Cortex-A processors with that of OMAP processors, highlighting the differences in memory hierarchy. [2]
j) What are the main architectural components of OMAP processors? [3]

PART – B

(50 Marks)

2.a) Discuss the register organization of the 8086 microprocessors, elaborating on the purposes and uses of its various types of registers.
b) Describe the concept of macros in 8086 assembly language programming. Provide examples of how macros are used to simplify coding and improve program efficiency. [5+5]

OR

3.a) Explain the physical memory organization in the 8086 architecture and detail the utilization of address lines for accessing physical memory.
b) Create a program demonstrating string manipulations in 8086 assembly language including operations such as string comparison, concatenation, and copying. [5+5]

4.a) Discuss the memory organization of the 8051 Microcontroller, detailing the types of memory and their significance in program execution.
b) Develop a program that sends a string of characters over UART using serial communication interrupts in the 8051. [5+5]

OR

5.a) Explore the instruction set of the 8051 Microcontroller, highlighting the different types of instructions and their functions in programming.

b) Describe the process of enabling and handling external hardware interrupts in the 8051 microcontroller. [5+5]

6.a) Discuss the steps involved in interfacing an external RAM module with the 8051 microcontroller, outlining the control signals and addressing schemes used.

b) Describe the role of the RS232 interface in establishing serial communication links between legacy devices and modern microcontrollers. [5+5]

OR

7.a) Illustrate the process of designing a keyboard interface with the 8051 microcontroller.

b) Analyze the key features of the I2C bus in facilitating communication between sensors, memory devices, and other peripherals on a shared bus. [5+5]

8.a) Discuss the fundamental features of ARM processors, highlighting the key characteristics that differentiate ARM architecture from other processor types.

b) Explain the role of registers in ARM architecture, detailing the different types of registers available, their functions, and the advantages. [5+5]

OR

9.a) Illustrate the handling of exceptions and interrupts in ARM architecture, explaining the role of the Interrupt Vector Table in mapping interrupt sources.

b) Introduce the Thumb instruction set in ARM architecture, highlighting its benefits in terms of code size efficiency and performance optimization. [5+5]

10.a) Explain the architectural components of ARM Cortex processors, including the instruction set architecture, pipelining structure, and memory hierarchy.

b) Discuss the architectural features of OMAP processors, including the integration of multiple processing cores and multimedia accelerators. [5+5]

OR

11.a) Provide an overview of the OMAP (Open Multimedia Applications Platform) processor family, highlighting its target applications

b) Describe the memory architecture of OMAP processors, including the integration of on-chip memory, cache hierarchy, and support for external memory interfaces. [5+5]

---ooOoo---