Code No: S9504 **RA**

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
B. Tech III Year I Semester Examinations, May - 2018
ELECTRONIC CIRCUITS
(Electrical and Electronics Engineering)

Time: 3 hours **Max. Marks: 75**

Answer any five questions
All questions carry equal marks
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1.a) Draw the circuits for the CE and CC amplifiers and explain the same.
b) For any transistor amplifier prove that Ri = hi/(1-$h_r A_V$). [9+6]

2.a) The input power to a device is 10,000W at a voltage of 1000V. The output power is 500W and the output impedance is 20Ω. (i) Find the power gain in decibels. (ii) Find the voltage gain in decibels. (iii) Explain why parts (i) and (ii) agree or disagree.
b) i) Calculate the overall voltage gain of four identical stages of an amplifier, each having a gain of 20.
ii) Calculate the overall upper 3-dB frequency for a four stage amplifier having an individual stage value of f_2 = 2.5 MHz.
c) Determine the cutoff frequencies for the circuit shown in figure 1 using the following parameters:
C_S = 10 µF, C_E = 20 µF, C_C = 1 µF, R_1 = 40 kΩ, R_2 = 10 kΩ, R_E = 2 kΩ, R_C = 4 kΩ, R_L= 2.2 kΩ, β = 100, r_0 = infinite Ω, V_{CC} = 20V. [5+3+7]

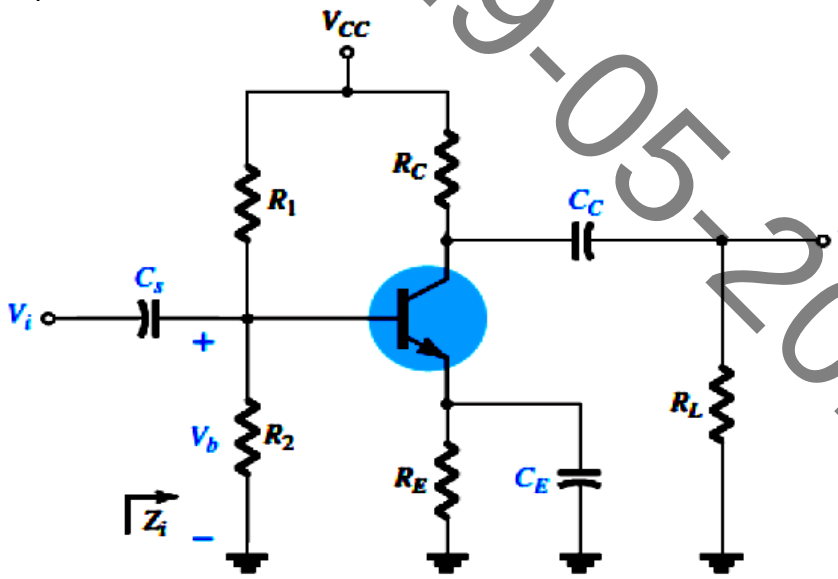

Figure 1

3.a) Describe with necessary derivations, the effect of negative feedback on the bandwidth and distortion in an amplifier.
b) The midband voltage gain of a certain amplifier is 500. Its upper half power frequency (f_2) is 20 kHz and the lower half –power frequency (f_1) is 20 Hz. What will be the upper and lower half power frequencies and voltage gain, if 2% negative feedback in introduced?

c) Calculate the gain with and without feedback for an FET amplifier as shown in figure 2 for circuit values R_1 = 800 kΩ, R_2 = 200Ω, R_o = 40 kΩ, R_D = 8 kΩ and g_m = 5000 µS. [5+5+5]

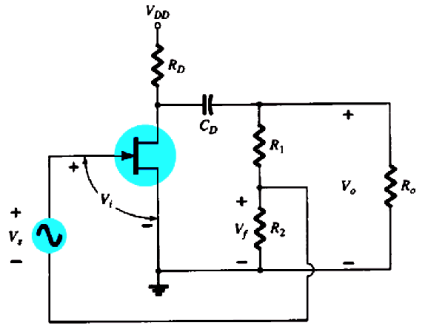

Figure 2

4.a) Explain briefly, What do you mean by an electronic oscillator? Give two applications of an oscillator.

b) Explain the operation of a transistorized Wien bridge oscillator with the help of neat circuit diagram. How is amplitude stability achieved in this circuit?

c) Explain with the neat circuit diagram, the working of a phase shift oscillator using three sections of RC network. State the expression for the frequency of oscillations and the minimum gain of the amplifier for sustained oscillations. [5+5+5]

5.a) Show how the response of a low pass RC circuit for square input for different time constant.

b) Show that the maximum collector efficiency of class –B amplifier is 78.6%.

c) For the circuit of figure 3, calculate the input power, output power and power handled by each output transistor and the circuit efficiency for an input of 12V rms. [5+5+5]

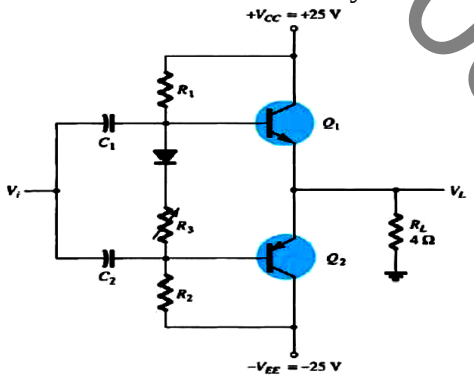

Figure 3

6.a) Explain the working of a transistor clipper in base clipping and peak clipping modes.

b) Design a clamper to perform the function indicated in figure 4.

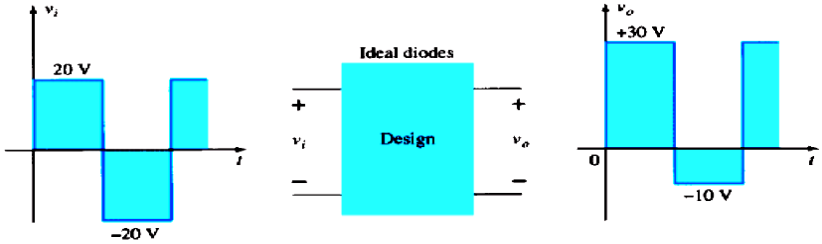

Figure 4

c) Describe the function of a double diode clipper. Define the difference between clipping and clamping circuits. [5+5+5]

7.a) Determine R_B and R_C for the transistor inverter of figure 5, if I_{Csat} = 10 mA.

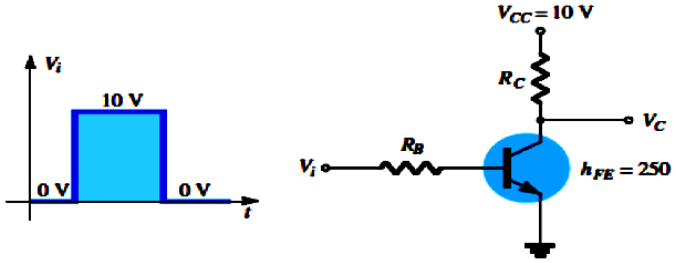

Figure 5

b) How would you provide temperature compensation for the Variations of V_{BE}?

c) Find the piecewise –linear equivalent circuit for the diode of figure 6. Use a straight line segment that intersects the horizontal axis at 0.7V and best approximates the curve for the region greater than 0.7V. [5+4+6]

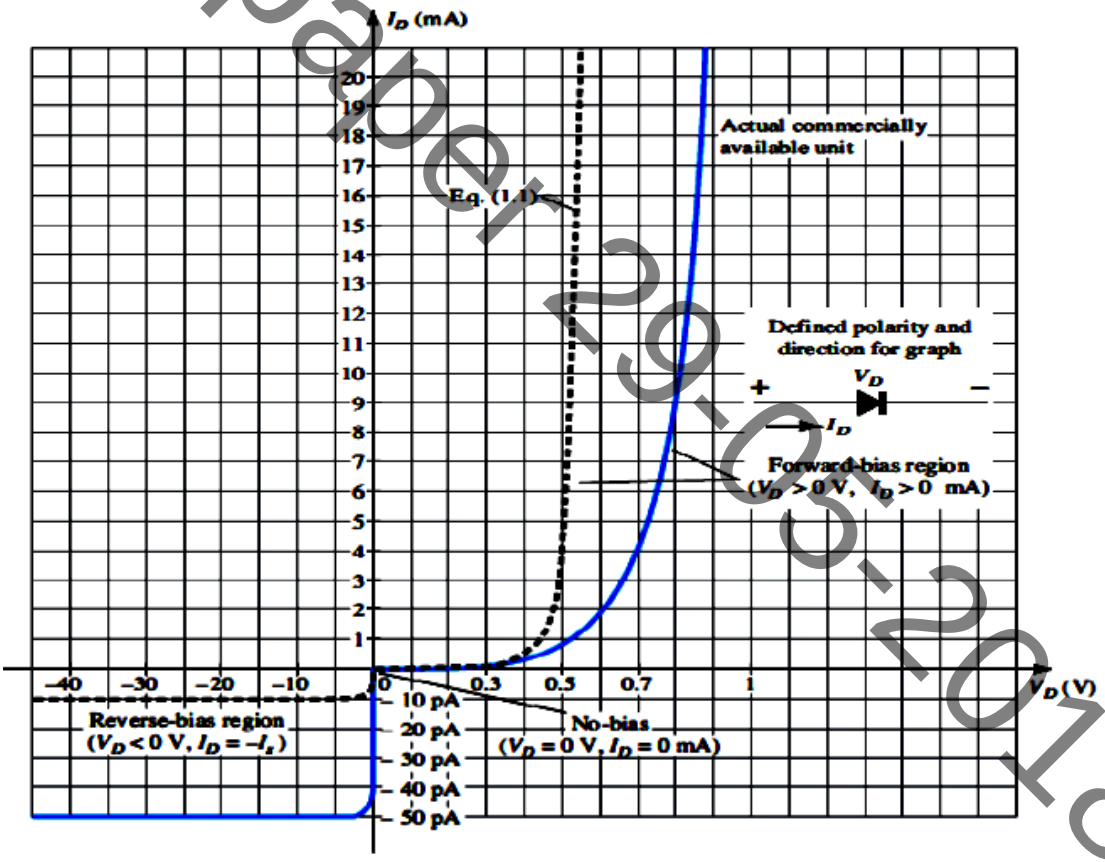

Figure 6

8.a) Explain the working of a collector coupled monostable multivibrator. Give expression for its gate width.

b) Draw and explain Bistable multivibrator circuit. [8+7]

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