Code No: 155SU **RA**

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
B. Tech III Year I Semester Examinations, January/February - 2023
DIGITAL SYSTEM DESIGN
(Electronics and Communication Engineering)

Time: 3 Hours **Max. Marks: 75**

Note: i) Question paper consists of Part A, Part B.
ii) Part A is compulsory, which carries 25 marks. In Part A, Answer all questions.
iii) In Part B, Answer any one question from each unit. Each question carries 10 marks and may have a, b as sub questions.

PART – A

(25 Marks)

1.a) Name different BCD codes. [2]
b) What is the base of the operation $\sqrt{41} = 5$? [3]
c) What is meant by Quad and Octet? [2]
d) What is a tie set Hazard? [3]
e) What is the drawback of SR Flip Flop? [2]
f) Obtain the characteristic equation of T Flip Flop. [3]
g) What is Mealy Machine? [2]
h) What is a Finite State Machine? [3]
i) Draw the DTL Logic diagram. [2]
j) What is the Noise Margin of standard TTL? [3]

PART – B

(50 Marks)

2.a) Express the following decimal numbers in 8421 code, XS-3 code, 2421 code and 5421 Code.
i) 429.5 ii) 807
b) Add the following in BCD and XS-3 codes:
i) 88.7+265.8 ii) 204.6 + 185.56 [5+5]

OR

3.a) Obtain the min and max terms of $A + B\bar{C} + AB\bar{D} + ABCD$.
b) Without reducing, convert the expression $(X\bar{Y} + X + \overline{X + Y})$ to NOR logic. [5+5]

4.a) Minimize and implement the following multiple output function in SOP form using K- Map $f_1 = \sum m(1,2,5,6,8,9,10)$ and $f_2 = \sum m(2,4,6,8,10,12,15)$.
b) Obtain the minimal POS expression using Quine McCluskey method for the Boolean function f = $\pi M(0,1,4,5,9,11,13,15,16,17,25,28,29,31).d(20,21,22,30)$. [5+5]

OR

5.a) Design a combinational circuit that accepts a three-bit number and generates an output binary number equal to the square of the input number.
b) Implement Boolean function F(A,B,C,D)=Σm(0,2,4,6,7,10,12) using 8:1 multiplexer. [5+5]

6.a) Design a SR flip flop using NAND gates. Explain the operation of the SR flip flop with the help of characteristic table.

b) Design T flip flop using SR flip flop and draw the timing diagram. [5+5]

OR

7.a) Describe shift registers and explain 4-bit bidirectional shift register with parallel load.

b) Design a MOD 6 up counter and verify whether it is Self-starting or not using JK flip flop. [5+5]

8.a) Design a sequence detector using D-Flip Flop to detect the sequence 11011.

b) The following pulse train is to be generated by using Shift Register. Design and draw logic diagram if the pulse train is

……1000100110101111…… [5+5]

OR

9.a) Design a Parity Generator and obtain the state table and state diagram. Realize the Parity Generator using D-Flip Flop.

b) Design Serial Binary Adder using D-Flip Flop. [5+5]

10.a) Explain about Transistor Logic.

b) Discuss the characteristics of I^2L. [5+5]

OR

11.a) Compare the Characteristics of various Logic Families.

b) Explain about Schottky TTL Logic Family. [5+5]

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